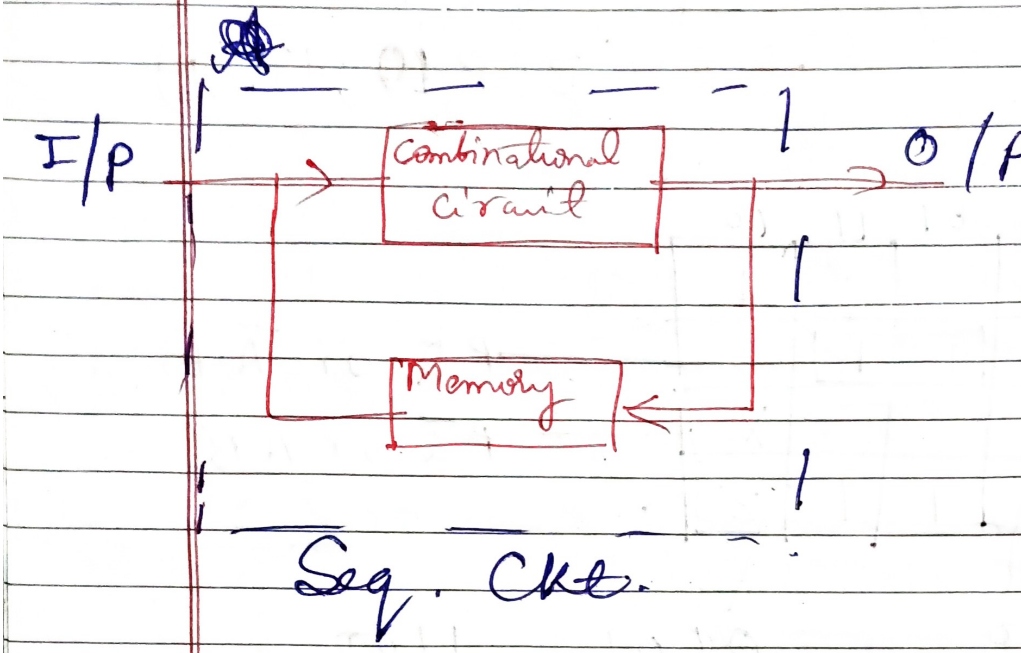
Sequential Circuits



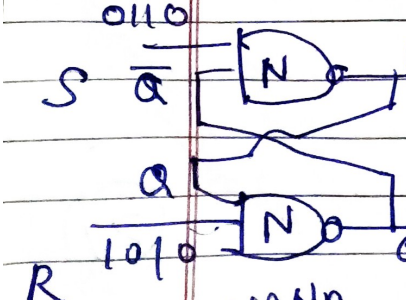
Seq. Ckt.

Seq. circuit is a combinational circuit with memory

O/P depends on present I/P & present state [Past O/P]

I/P	Present (Q_n)	Next (Q_{n+1})

Latches: (SR) (Nand Gate)



NAND

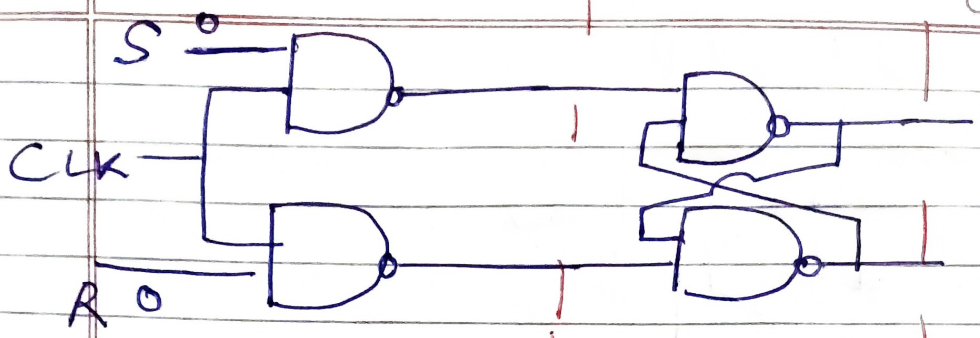
$1 \cdot \bar{Q} = \bar{1} + \bar{Q} = 0 + Q$

$\bar{1} \cdot Q = 0 + \bar{Q}$

S	R	Q_{n+1}
0	0	Invalid
0	1	1
1	0	0
1	1	Hold

Q4

SR Flip-flop



0 0 → Invalid
0 1 → 1
1 0 → 0
1 1 → Hold.

Truth Table

CLK	S	R	Q_{n+1}	
0	—	—	Q_n	Previous state
1	0	0	Hold	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	Invalid	Invalid.

Characteristics table

S	R	Q(n)	Q(n+1)	
0	0	0	0	Hold
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	X	Invalid
1	1	1	X	

S	R	
0	0	H
0	1	1
1	0	0
1	1	Inv.

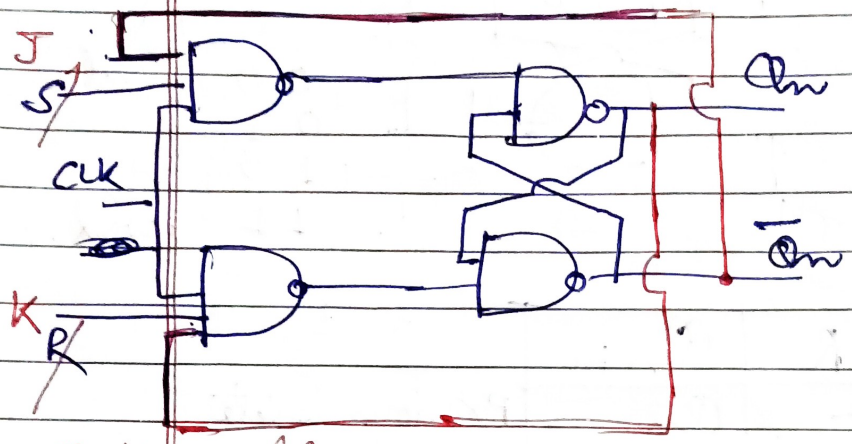
S \ $R\bar{Q}_n$	$R\bar{Q}_n$	RQ_n	RQ_n	$R\bar{Q}_n$
$\bar{S}$		1		
S	1	1	X	X

$Q_{n+1} = S + \bar{R}Q_n$

Excitation Table

Q(n)	Q(n+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

J-K Flip flop



S	R	Q_{n+1}
0	0	H
0	1	0
1	0	1
1	1	Invalid

Truth Table

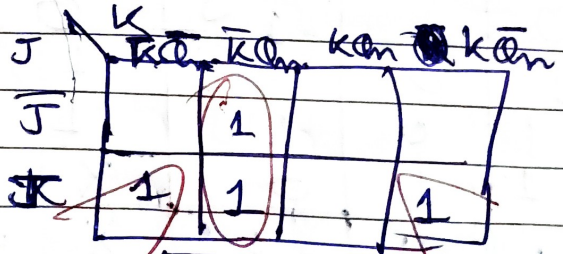
CLK	J	K	Q_{n+1}	
1	0	0	$H(Q_n)$	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\bar{Q}_n$	Toggle

let us suppose $Q_n = 1$ $Q_{n+1} = 0$

$Q_n = 0$ $Q_{n+1} = 1$

Characteristic Table

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

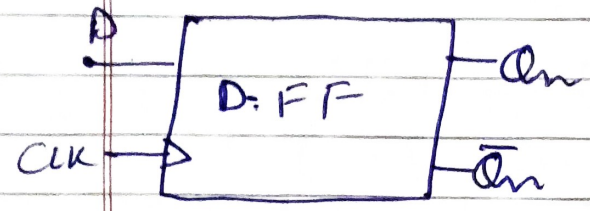


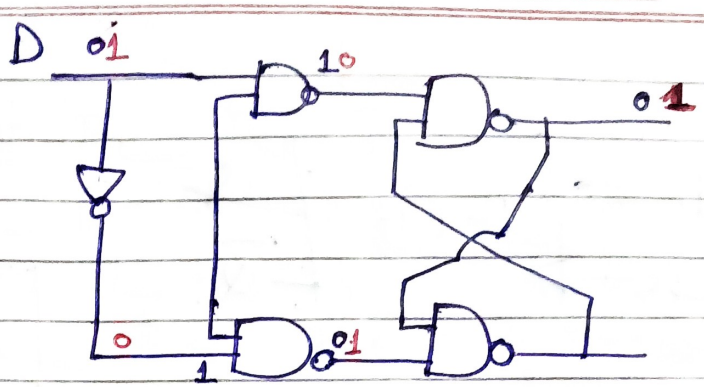
$Q_{n+1} = \bar{K}Q_n + J\bar{Q}_n$

Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D-FF





Using SR

S	R	Qn+1
0	0	Inv.
0	1	1
1	0	0
1	1	Hold

Truth Table

D	Qn+1
0	0
1	1

Characteristic Table

D	Qn	Qn+1
0	0	0
0	1	0
1	0	1
1	1	1

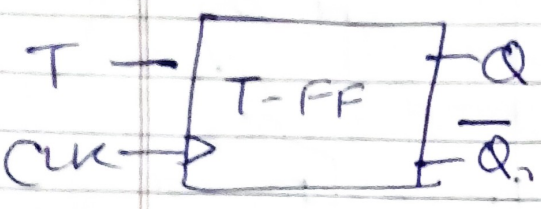
Characteristic eqn.

$$Q_{n+1} = D$$

Excitation table

Qn	Qn+1	D
0	0	0
0	1	1
1	0	0
1	1	1

T-FF



Truth Table

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

Characteristic Table

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic eqn. $Q_{n+1} = T \oplus Q_n$

Excitation Table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Q_A	Q_{A+1}	S	R	J	K	D	T
0	0	0	X	0	X	0	0
0	1	1	0	1	X	1	1
1	0	0	1	X	1	0	1
1	1	X	0	X	0	1	0

Counters

- Synchronous
- Asynchronous.

Sequential circuit - Output depends on present I/P & Past O/P.

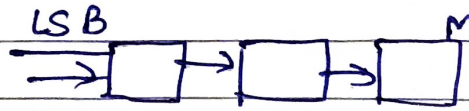
Counters - A sequential circuit that goes through a sequence of states upon application of clock pulse It stores/displays sequences of states due to clock.

A n-bit counter has n-FFs.
A n-bit counter has 2^n states.
States :- 0 - $(2^n - 1)$ by using n FFs.

Mod N-Counter

N = no. of states (MOD no. / modulus count)

$N \leq 2^n$



MOD 8 ⇒ no. of states & CLK

$N \leq 2^n \Rightarrow 8 \leq 2^n \Rightarrow n = 3 =$ no. of FF

Applications

(FSM) Finite State Machine - Synchronous Seq. Circuit (VLSI)
FPGA - Field Programmable Gate Arrays.
ASIC - Application Specific Integrated Circuits ①
ASIC - is designed for specific application while FPGA is a multipurpose microchip that one can reprogram for multiple applications