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Counters

- Synchronous
- Asynchronous.

Sequential circuit - Output depends on present I/P & Past O/P.

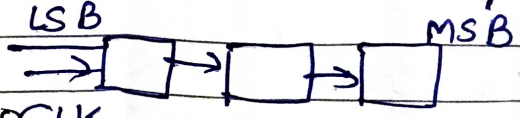
Counters - A sequential circuit that goes through a sequence of states upon application of clock pulse. It stores/displays sequences of states due to clock.

A n-bit counter has n-FFs.
A n-bit counter has 2^n states.
States :- 0 - $(2^n - 1)$ by using n FFs.

Mod N-Counter

N = no. of states (MOD no. / modulus count)

$N \leq 2^n$



MOD 8 ⇒ no. of states 8 CLK

$N \leq 2^n \Rightarrow 8 \leq 2^n \Rightarrow n = 3 =$ no. of FF

Applications

(FSM) Finite State Machine - Synchronous Seq. Circuit (Vlsi)
FPGA - Field Programmable Gate Arrays.
ASIC - Application Specific Integrated Circuits
ASIC - is designed for specific application while FPGA is a multipurpose microchip that one can reprogram for multiple applications

Ring Counter

No. of mod = No. of states

$n = 4 =$ no. of FF

no. of unused states $= 2^n - n$

Johnson Counter

No of states used $= 2^n = 16$

No. of states unused $= 2^n - 2n = 8$

Useable states $= 2n = 8$

Asynchronous Counter - Counting will be pattern (up or down)

Synchronous Counter - Random Counting possible.

BCD Counter
Binary Counter
Decade Counter
10-bit Counter / Mod-10 Counter

CLK (↑) ⇒ $\overline{Q}$ Out] up (opposite)

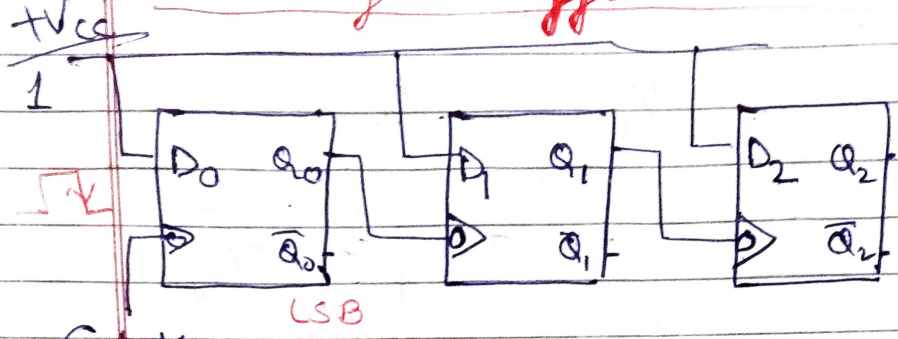
CLK (↓) ⇒ Q out] down (same) (2)

Nature same → down
different → up.

$\overline{Q}$ → -ve ↓↓

Q → -ve ↑↑

-ve Edge Trigger UP Counter/Ripple Counter



$$F_{out} = \frac{F_{in}}{8}$$

Ripple = I/P Clock pulse for II & III FF is the O/P of their previous FFs.

In ripple counter, Q_0 toggle for every clock pulse -ve edge.

Q_1 toggles, $Q_0 \longrightarrow$ 1 to 0

Q_2 " , $Q_1 \longrightarrow$ 1 to 0

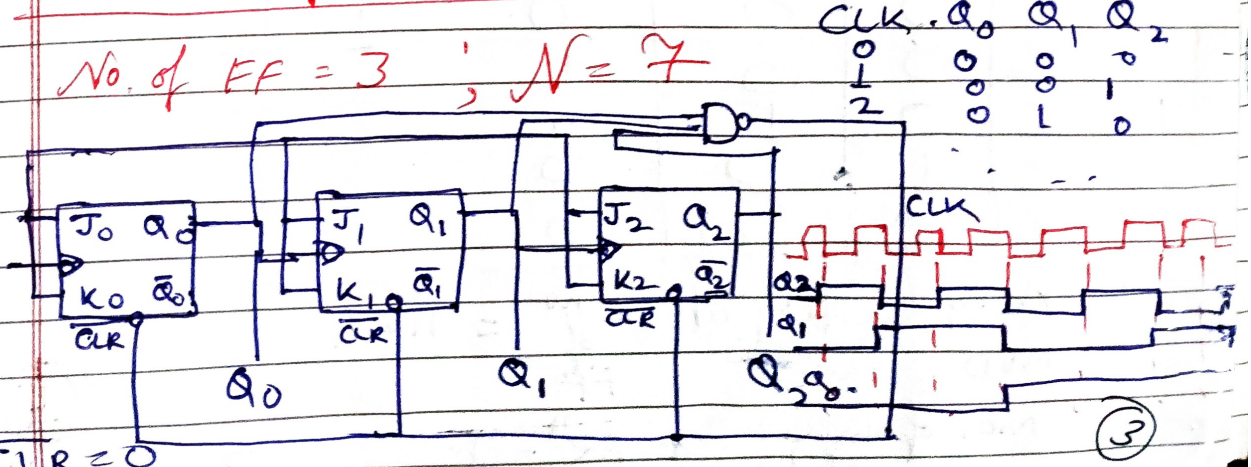
Q_0 " , for only -ve edge.

	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	0	0	0
8	0	0	0

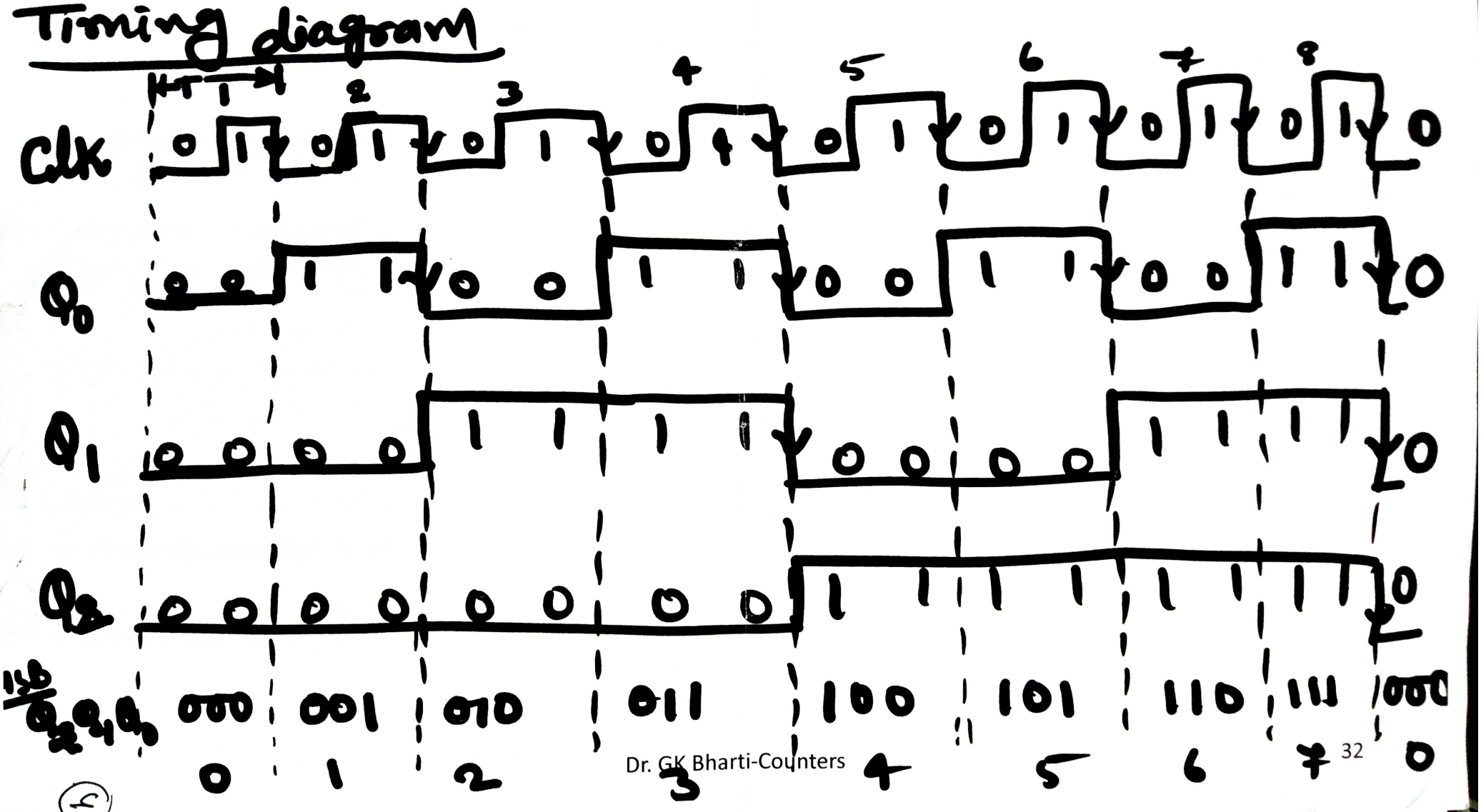
MOD-7 Ripple Counter

No. of FF = 3 ; N = 7

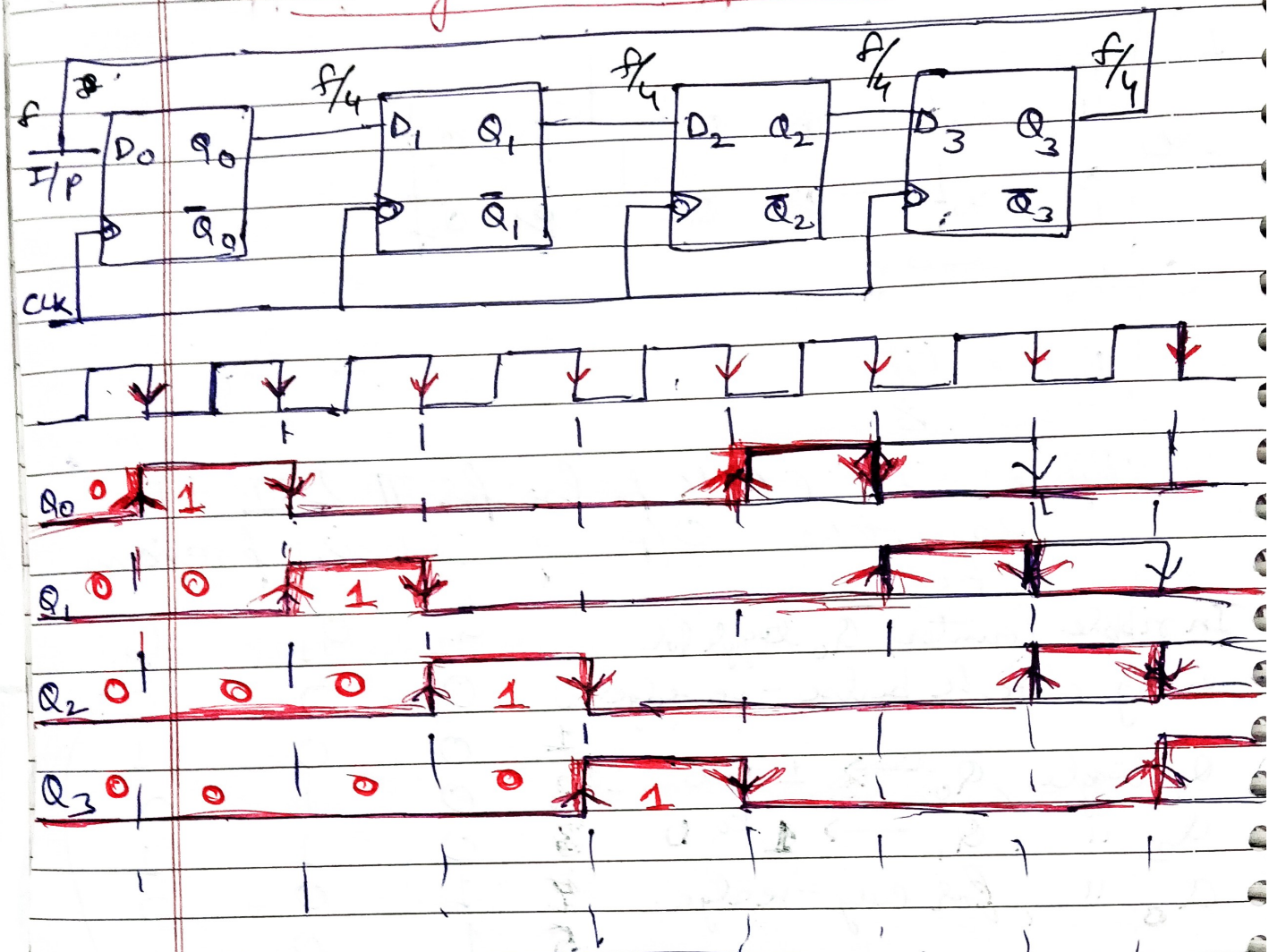
CLK	Q_0	Q_1	Q_2
0	0	0	0
1	0	0	1
2	0	1	0
	0	1	1
	1	0	0
	1	0	1
	1	1	0



Timing diagram



Ring Counter

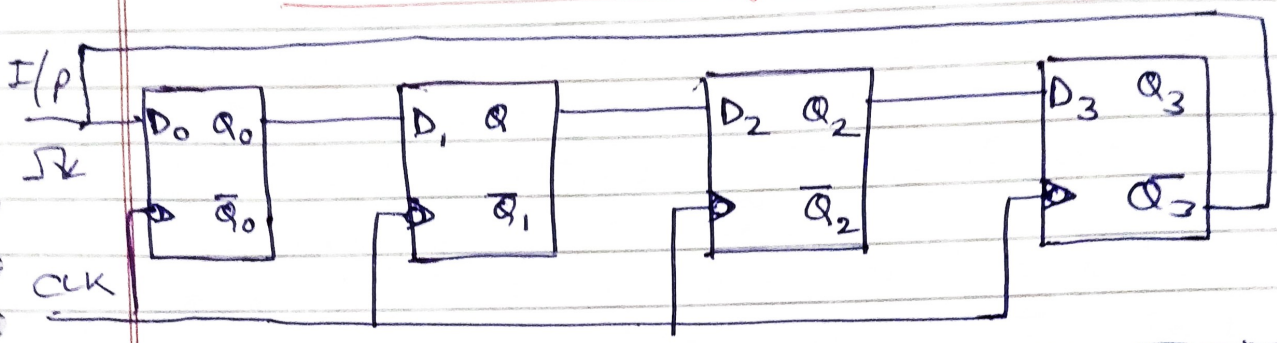


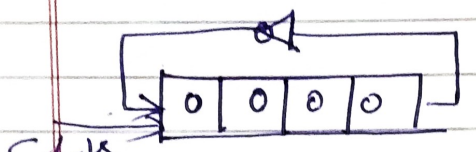
Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	1	0	0
1	0	0	0
0	0	0	1

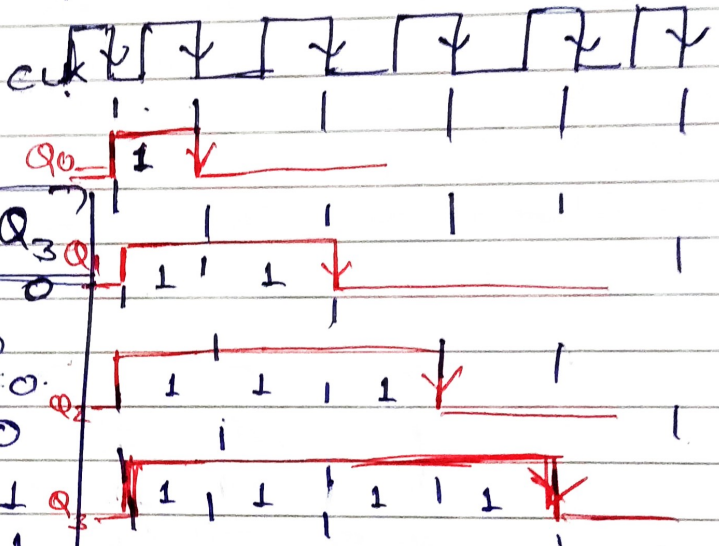
No. of MOD = 2 No. of states − No. of FF = n = 4

No. of unused states = $2^n - n$

Twisted Ring Counter



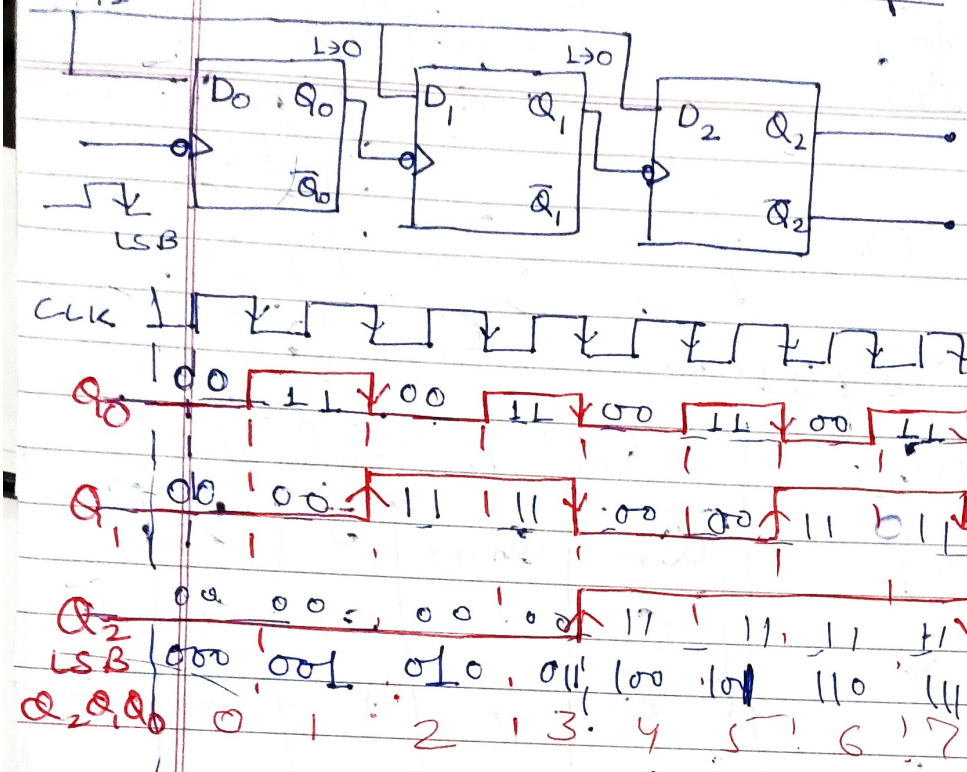




CLK	Q_0	Q_1	Q_2	Q_3
	0	0	0	0
1st	1	0	0	0
2nd	1	1	0	0
3rd	1	1	1	0
4th	1	1	1	1
5th	0	1	1	1
6th	0	0	1	1
7th	0	0	0	1
8th	0	0	0	0

Synchronous — Switch of Clock pulse is ON (Latch) but not giving clock signal that's why it is fast.

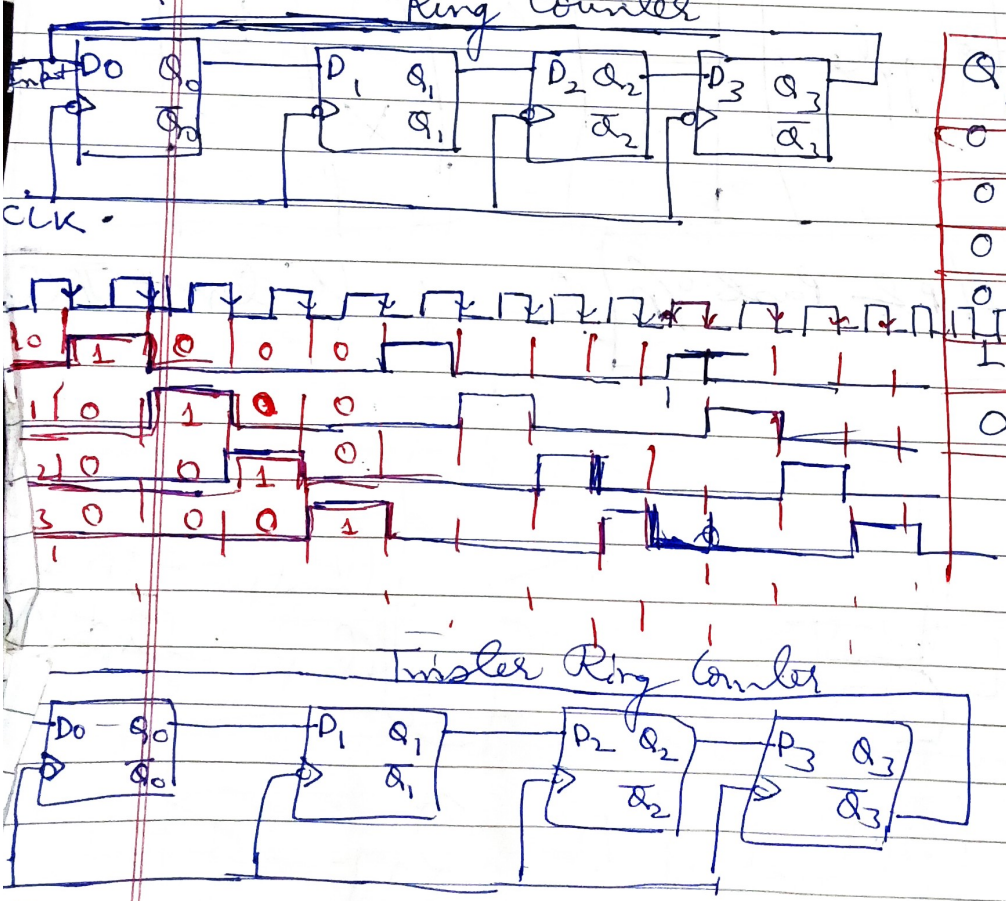
3 bit ripple Counter:



$2^3 = 8$

CLK	Q_2	Q_1
0	0	0
1	0	0
2	0	1
3	0	1
4	1	0
5	1	0
6	1	1
7	1	1
8	0	0

Ring Counter



Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	1	0	0
1	0	0	0
0	0	0	1

Twisted Ring Counter

Design a synchronous counter with counting sequence 0, 2, 1, 3, 0.

Soln:-

i) Identify no. of states & no. of FFs
ii) Construct state table
iii) Write excitation eqn.
iv) Minimize logical expression
v) Implement

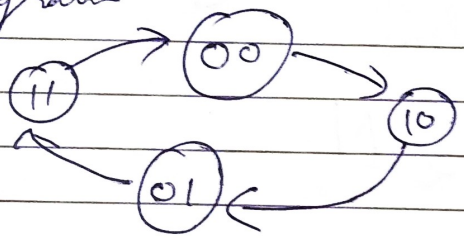
Sequence

$0 \rightarrow 2 \rightarrow 1 \rightarrow 3 \rightarrow 0$

00 10 01 11

No. of FFs = (11) ⇒ 2

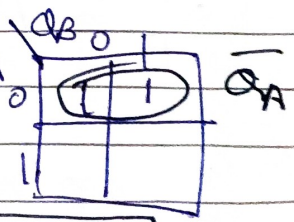
State Diagram



State table:

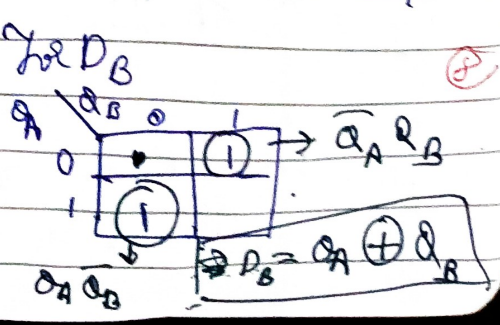
Present state		Next State		Excitation	
Q_A	Q_B	Q_{A+1}	Q_{B+1}	D_A	D_B
0	0	1	0	1	0
1	0	0	1	0	1
0	1	1	1	1	1
1	1	0	0	0	0

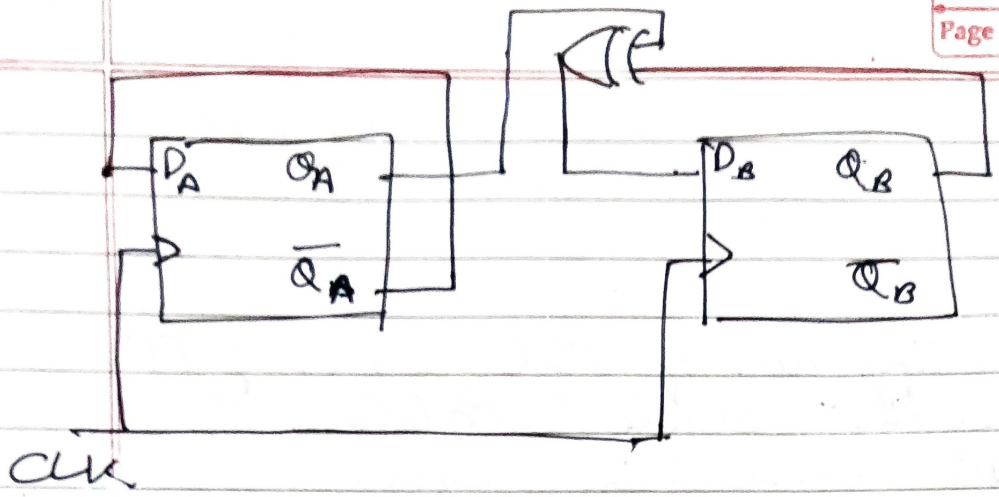
Eqn for D_A



⇒ $D_A = \bar{Q}_A$

For D_B





Circuit Diagram

Important Points:

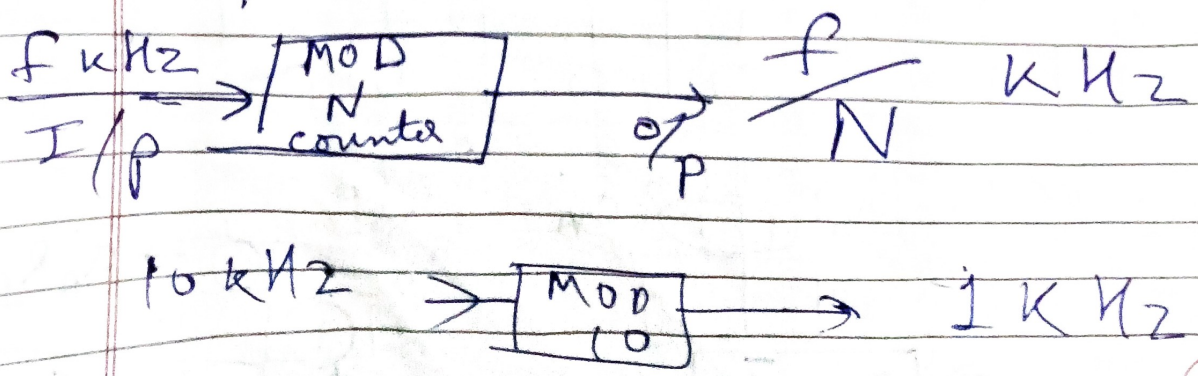
N = no of states $\leq 2^n$
= modulus

$n \geq \log_2 N$

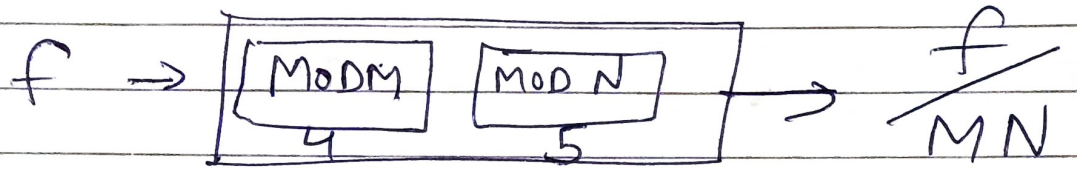
MOD 15 ⇒ no. of states = 15

$15 \leq 2^n \Rightarrow n = 4$

Freq. divider



If MOD M & MOD N Counters are Cascaded



4 X 5 = 20 MOD