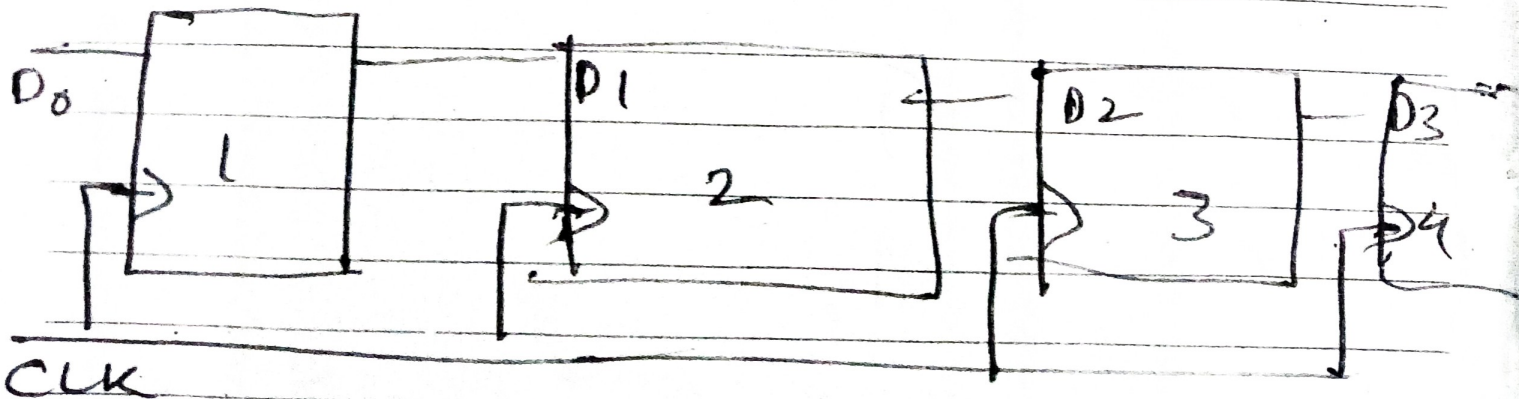


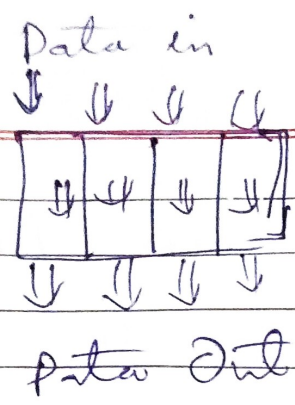
Shift Register

- ✓ A set of n - flip flop
 - Each flip-flop stores one bit.
- ✓ Two basic functions
 - ↳ Data Storage
 - ↳ Data transfer

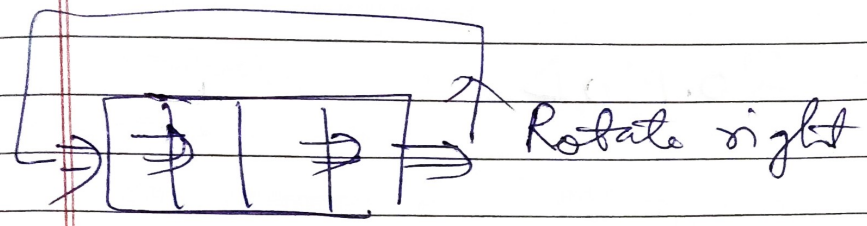
Shift register is a type of sequential logic circuit, mainly for storage of digital data.

They are a group of FFs connected in a chain so that output from one FFs ~~connected~~ in a become the input of next FF.



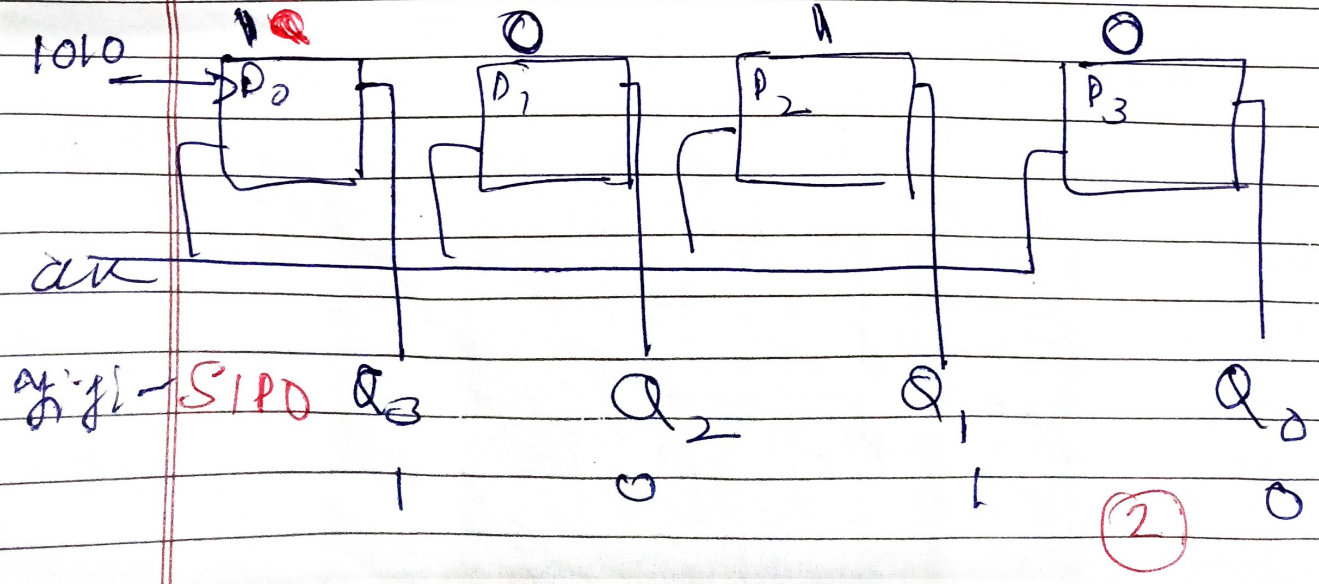


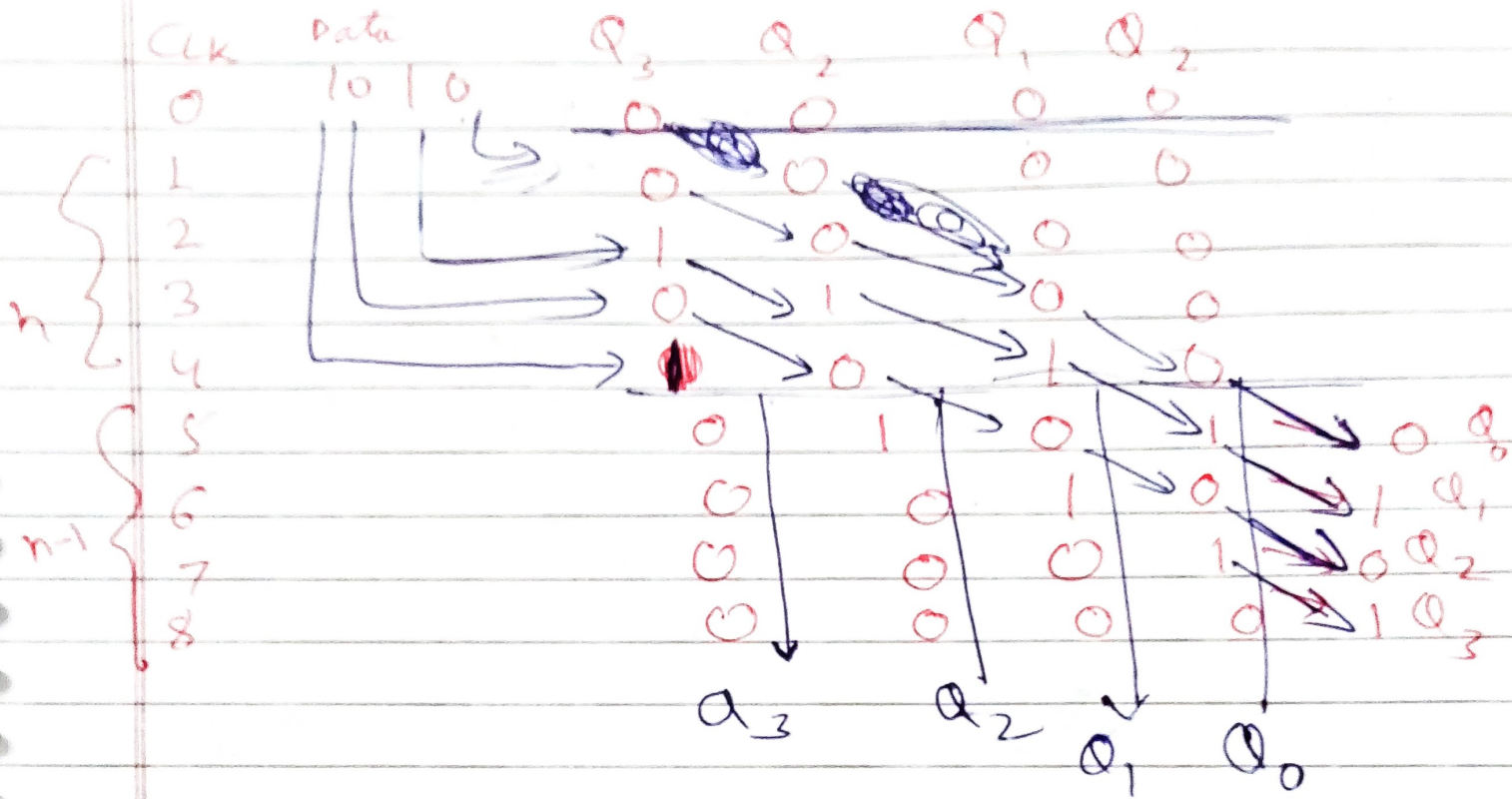
(Parallel in Parallel Out)



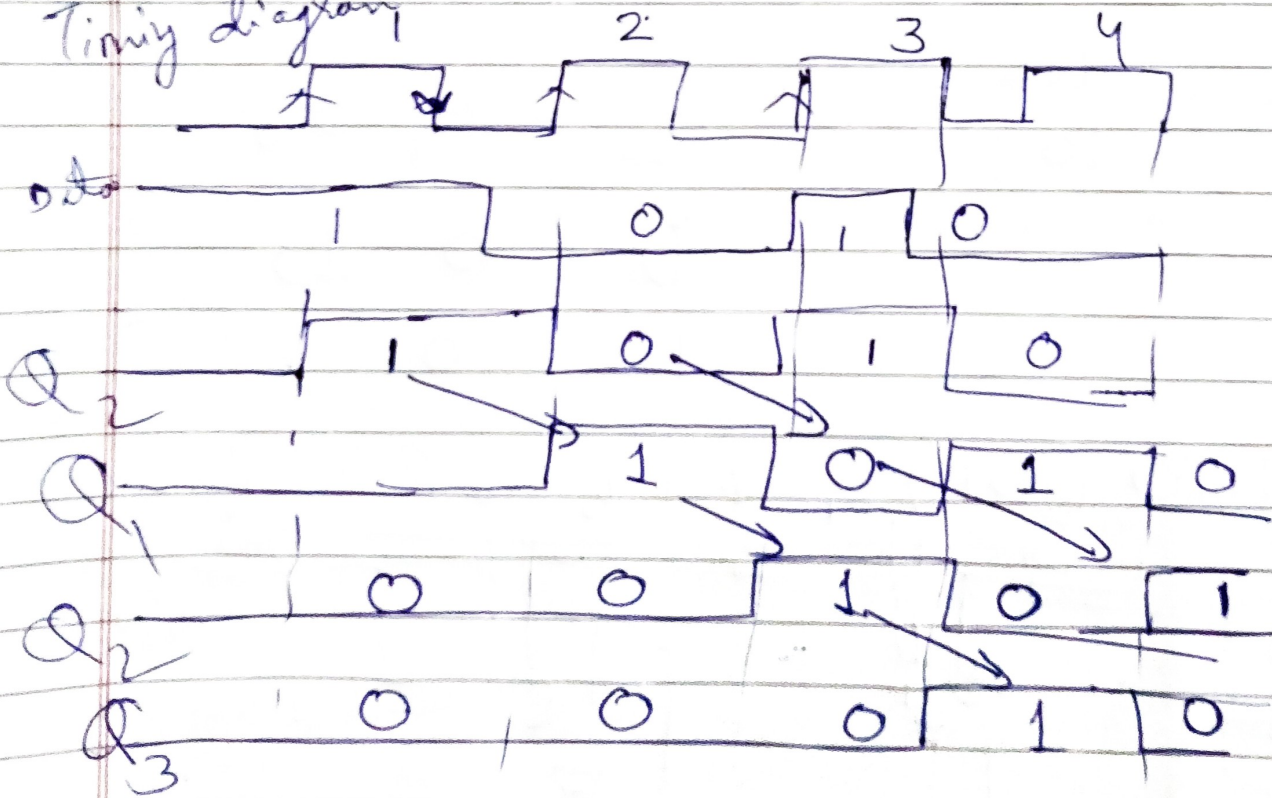
Types of Shift Register

- i) SISO
- ii) SIPO
- iii) PISO
- iv) PIPO
- v) Bidirectional Shift Register
- vi) Universal Shift Register



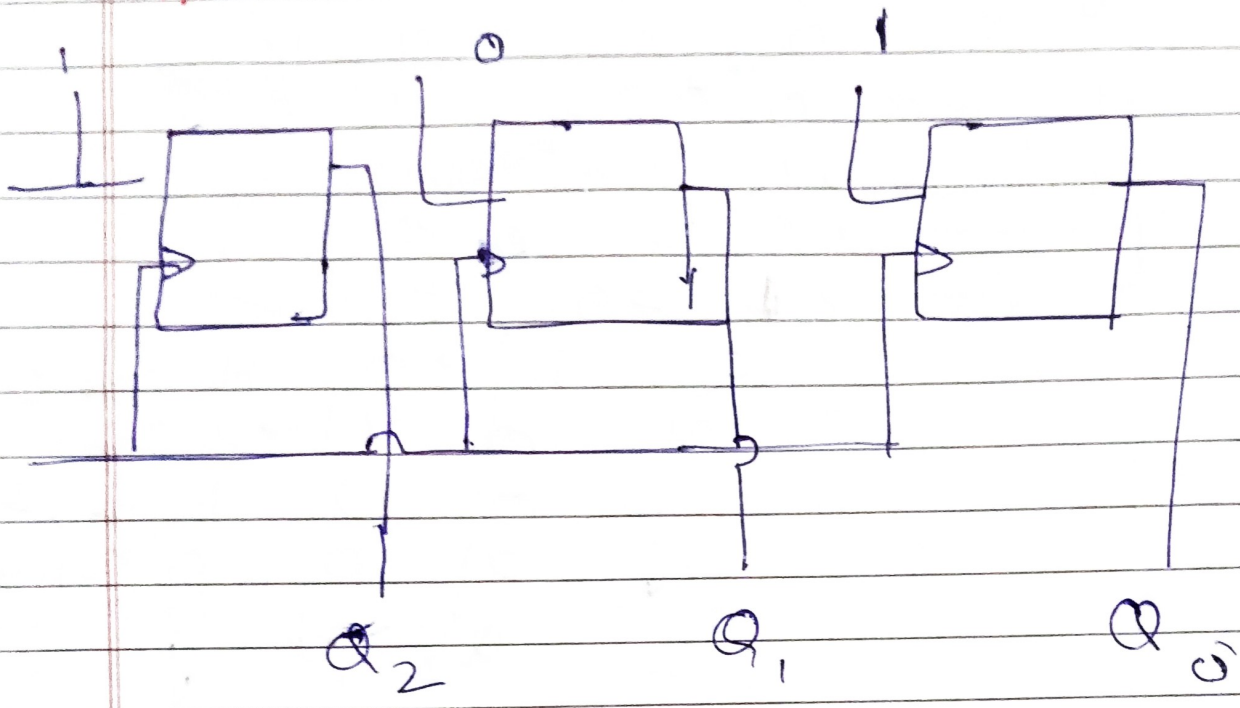


Timing diagram



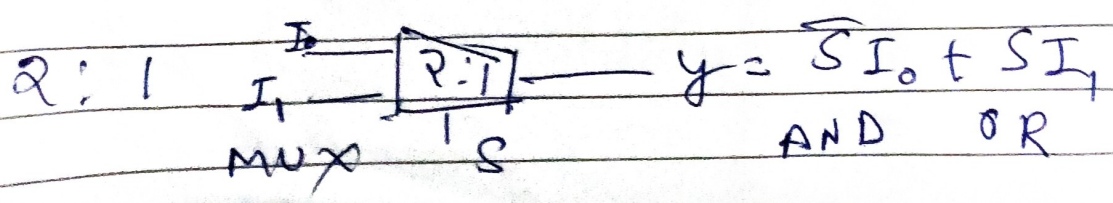
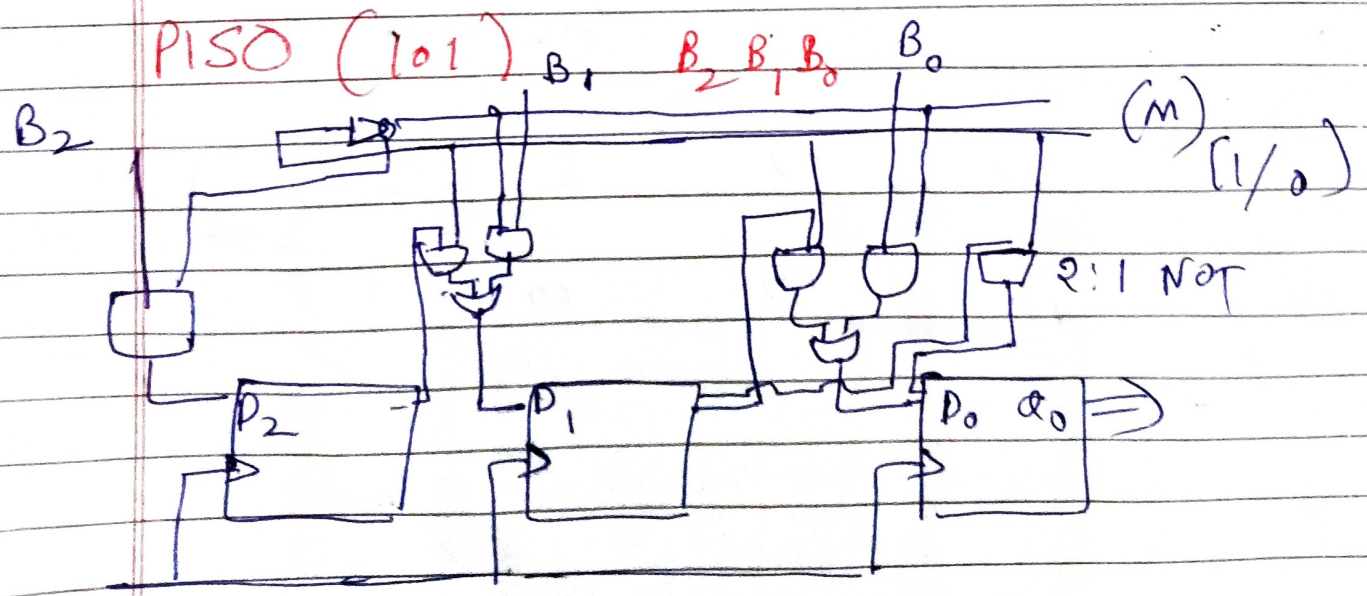
3

PIPO (101)



| CLK | Data | Q ₂ | Q ₁ | Q ₀ |
|-----|------|----------------|----------------|----------------|
| 0 | 101 | 0 | 0 | 0 |
| 1 | | 1 | 0 | 1 |

PISO (101)



(4)

| | No. of Clock Pulse | Data Out |
|------|--------------------|----------|
| SISO | 1 | 1 |
| SIPO | n | n-1 |
| PISO | 1 | 0 |
| PIPO | 1 | n-1 |

Imp. Questions (for Practice)

Q. Design Syn Counter with Counting Seq 0, 2, 1, 3, 4, 0

Soln:-

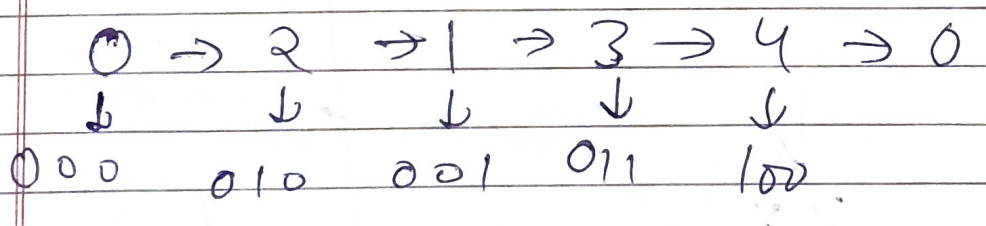
→ Identify no. of states $\Rightarrow n = 3$
& no. of FFs = 3

→ Construct State Table

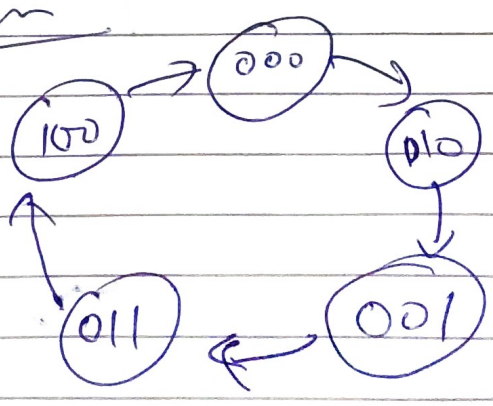
→ Write Excitation eqn

→ Minimize Logical Expression

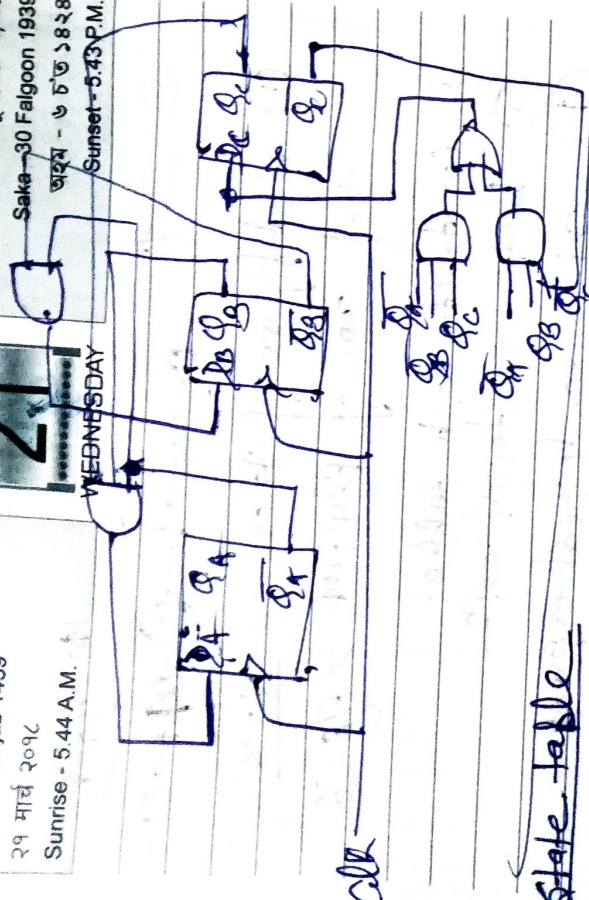
→ Implement



State Diagram



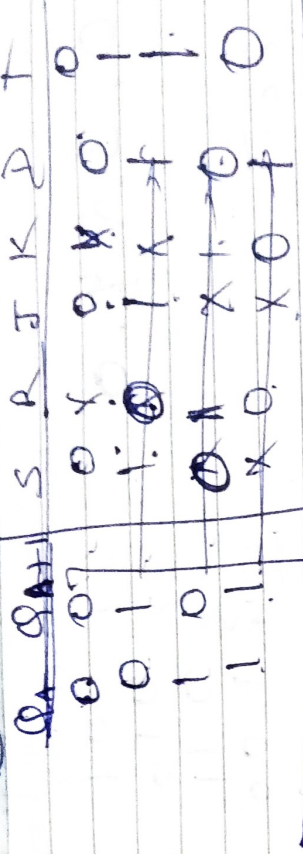
5



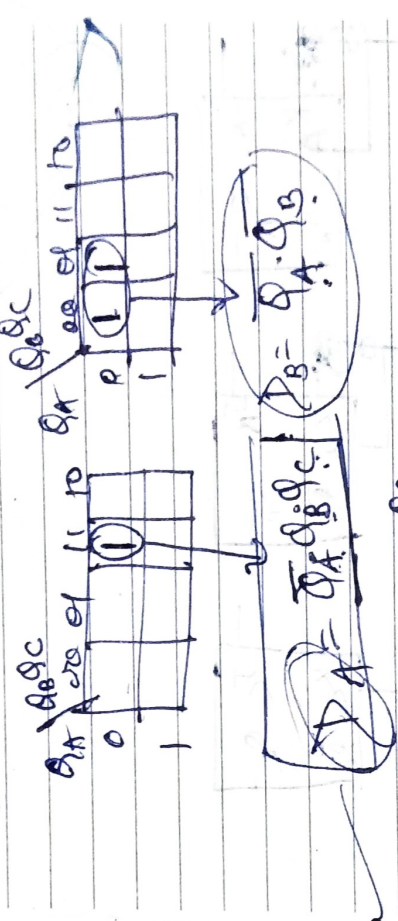
State table

| Present state QA QB QC | Next state QA QB QC | Excitation table DA DB DC |
|---------------------------|------------------------|------------------------------|
| 0 0 0 | 0 1 0 | 0 1 0 |
| 0 1 0 | 0 0 1 | 0 0 1 |
| 0 0 1 | 0 1 1 | 0 1 1 |
| 0 1 1 | 1 0 0 | 1 0 0 |
| 1 0 0 | 0 0 0 | 0 0 0 |

(6)



for DA
DB



(7)

