Digital System Design EC 503

Digital System Design Implementation

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ASIC vs IC

- **Standard ICs**
  - ICs sold as Standard Parts
  - An Integrated Circuit is made of silicon that can store data using analog or digital technology. Standard Integrated Circuit is ideal for small series
- **Application Specific Integrated Circuits(ASIC)**
  - It s a chip customized for a specific use.
  - A modern ASIC chip contains microprocessors, RAM, ROM, memory blocks, and flash memory.
  - Design can also be tailored to meet the specific requirements for a product
  - Useful in the production of consumer electronics and products that are widely used.
  - Reduced Cost and Improved Reliability

Types of ASICs

- Full-Custom Ics/Fixed ASICs and Programmable ASICs

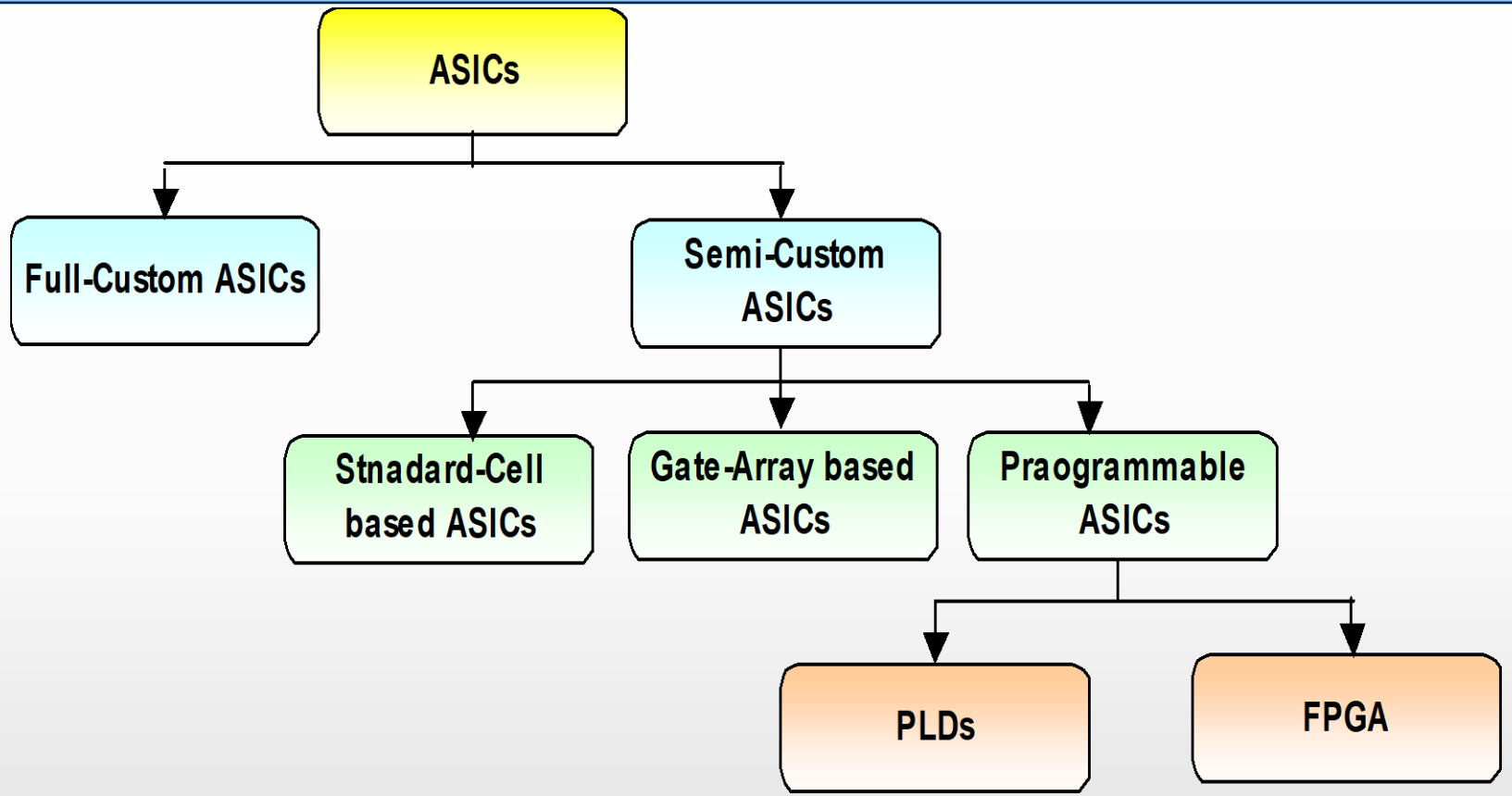
➢**Wafer:** A circular piece of pure silicon

➢**Wafer Lot:** 5~30 wafers, each containing hundreds of chips(dies) depending upon size of the die

➢**Die:** A rectangular piece of silicon that contains one IC design

➢**Mask Layers:** Each IC is manufactured with successive mask layers(10-15 layers)

ASICs Types



Full-Custom ASICs: Possibly all logic cells and all mask layers customized

Semi-Custom ASICs: all logic cells are pre-designed and some (possibly all) mask layers customized

Full Custom ASIC

- A Full custom is one which includes some (possibly all) logic cells that are customized and all mask layers that are customized.
- A microprocessor is an example of a full-custom IC. Designers spend many hours squeezing the most out of every last square of microprocessor chip space by hand.
- Customizing all of the IC features in the allows designers to include analog circuits, optimized memory cells, or mechanical structures on an, for example. Full custom ICs are the most expensive to manufacture and to design.
- The specialized full-custom ICs are often intended for a specific application so, we might call some of them as full-custom ASICs.
- In a full-custom ASIC an engineer designs some or all of the logic cells, circuits, or layout specifically for one ASIC. This means the designer avoids using pretested and pre characterized cells for all or part of that design.

Gate Array Based ASIC

- This is a type of Semicustom ASICs.
- The transistors are predefined on the silicon wafer
- The predefined pattern of transistors on a gate array is the best array, and the smallest element that is replicated to make the base array is the base cell.
- Only top few layers of metal, which define the interconnect between transistors, are defined by the designer using custom masks. To distinguish this type of gate array from other types of gate array, it is often called a masked gate array(MGA).
- The logic cells in a gate-array library are often called macros. The reason for this is that the base-cell layout is the same for each logic cell, and only the interconnect is customized, which is similar to a software macro

Types of Gate-array based ASICs

- There are three types of Gate Array based ASICs.
- Channelled gate arrays.
- Channel less gate arrays.
- Structured gate arrays.

➢ Channelled gate arrays: The Channelled gate array was the first to be developed. In a channelled gate array space is left between the rows of transistors for wiring.

➢Features of Gate-array based ASICs

- Only the interconnect is customized.
- The interconnect uses predefined spaces between rows of base cells
- Manufacturing lead time is between two days and two weeks,

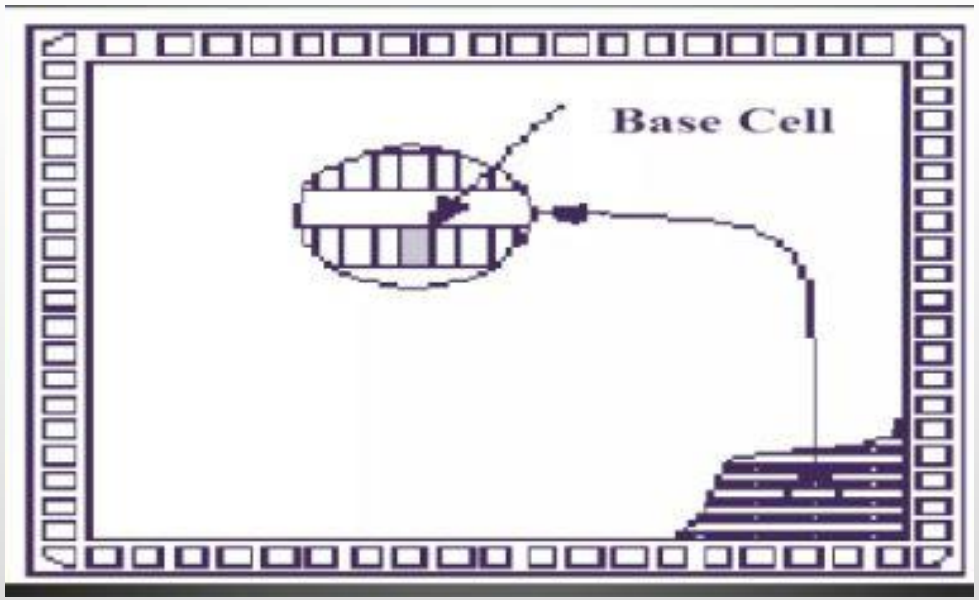


Fig: A channelled gate-array die

Channel less Gate Array

- This channel less gate-array architecture is now more widely used.; The routing on a channel less gate array uses rows of unused transistor.
  - The key difference between channel less and channelled gate array is there is no predefined areas set aside for routing between cells on a channel less gate array. Instead we route over the top of the gate array devices.
  - We can do this because we customize the contact layer that defines the connections between metal 1, the first layer of metal, and the transistors.

➢Features of Channel less Gate Array:

- Only the interconnect is customized
- Interconnect uses predefined spaces between rows of base cells.
- When we use an area of transistor for routing in a channel less array, we do not make any contacts to the devices lying underneath , we simply leave the transistors unused.

- The basic difference between a channel less gate array and channelled gate array is that there are no predefined areas set aside for routing between cells on a channel less gate array. Instead we route over top of the gate array devices.

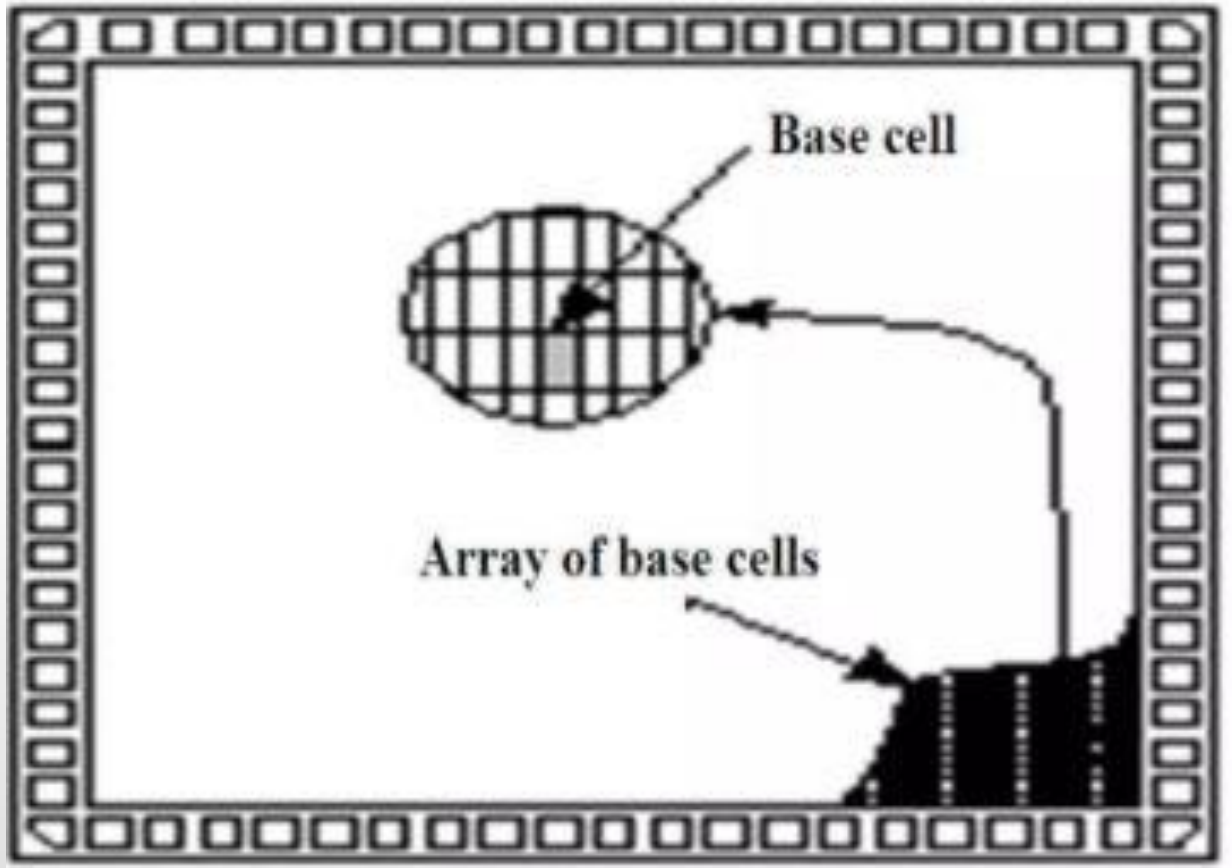


Fig: A channel less gate-array die

Structured Gate Array

- This design combines some of the features of Cell based ASIC(CBICs) and MGAs(Masked Gate Array) .It is also known as embedded gate array or structured gate array or master slice or also called as master image.
- One of the limitations of the MGA is the fixed gate array base cell. This makes the implementation of memory, difficult and inefficient.
- In an embedded gate array some of the IC area is set aside and dedicate it to a specific function. This embedded area either can contain a different base cell that is more suitable for building memory cells, or it can contain a complete circuit block, such as a microcontroller.

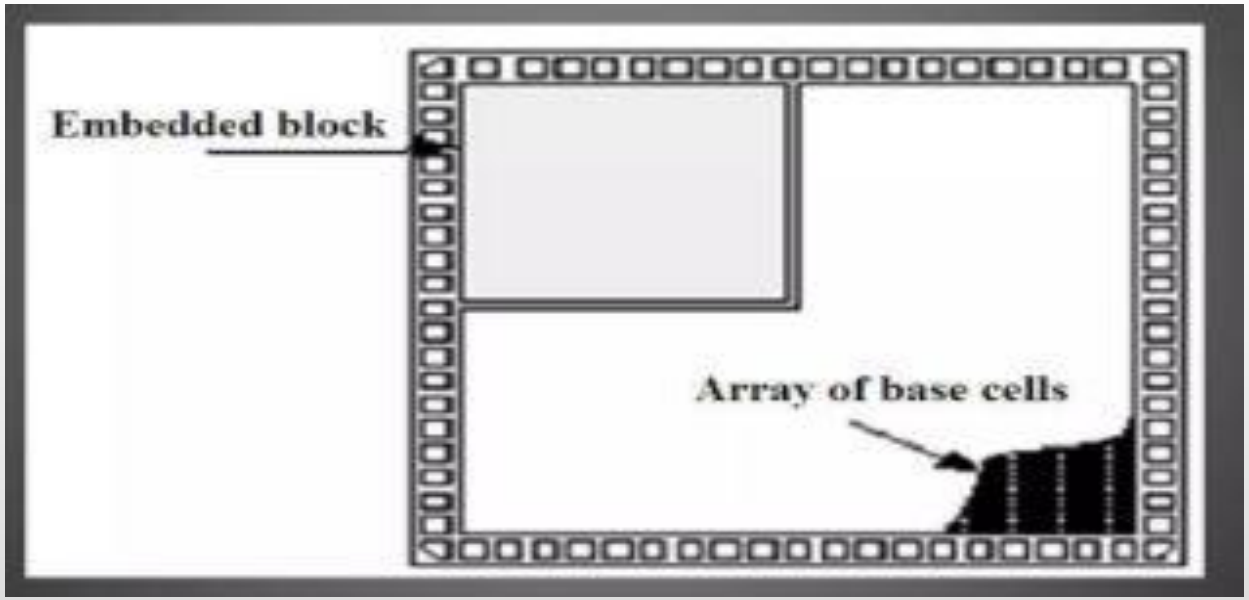


Fig: A structured or embedded gate-array die showing an embedded block in the upper left corner

Features of Structured Gate Array

- Only the interconnect is customized.
- Custom blocks (the same for each design) can be embedded.
- An embedded gate array gives the improved area efficiency and increased performance of a CBIC but with the lower cost and faster turn around of an MGA.
- The disadvantage of an embedded gate array is that the embedded function is fixed.

Thank You