Digital System Design EC 503

Application Specific Integrated Circuit

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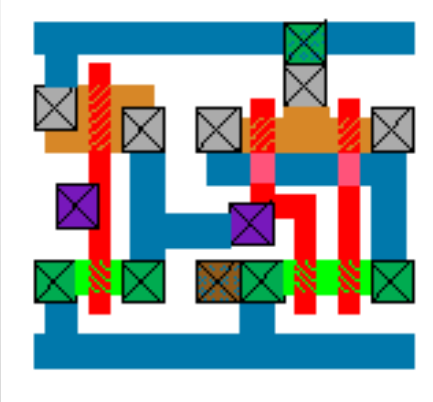
Introduction to ASIC

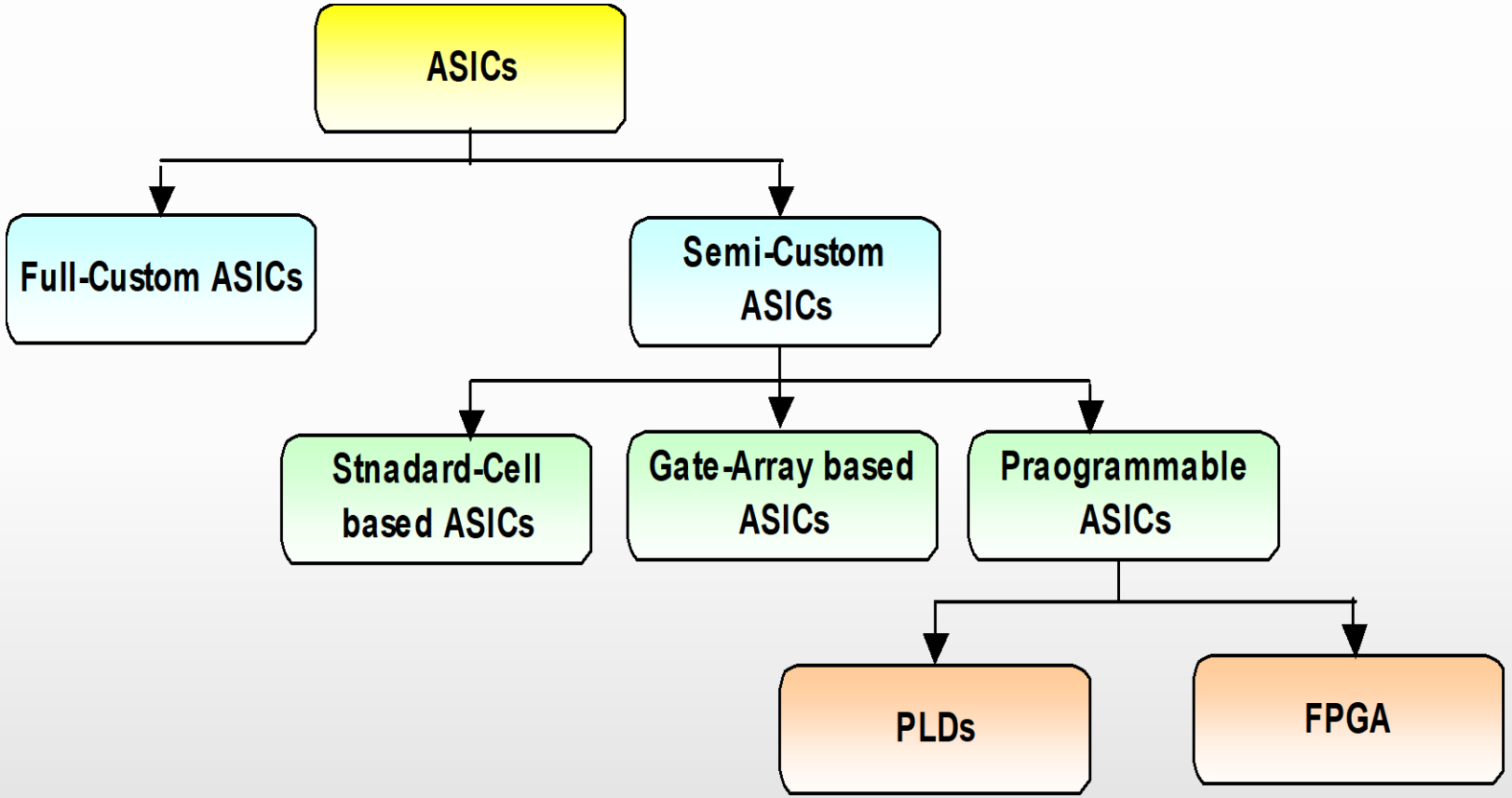
- ASICs are custom-designed integrated circuits developed to meet specific application requirements.
- ASICs offer tailored solutions for applications with unique performance, power, and size constraints, surpassing the limitations of off-the-shelf components.
- ASICs provide optimized performance, reduced power consumption, smaller form factors, and enhanced functionality compared to generic integrated circuits.



ASIC Design Process

- Overview of the ASIC design flow: The ASIC design process involves several stages, including requirements analysis, architecture design, RTL (Register Transfer Level) design, verification, synthesis, and fabrication.
- Steps involved: Designers collaborate closely with clients to understand the application requirements thoroughly. They then proceed with architectural and RTL design, followed by rigorous verification to ensure correctness and reliability. Synthesis transforms the RTL code into a netlist, which is then fabricated into silicon chips.
- Importance of collaboration between designers and customers: Close collaboration ensures that the ASIC meets the specific needs of the application, leading to successful implementation and deployment.

ASICs Types



Full-Custom ASICs: Possibly all logic cells and all mask layers customized

Semi-Custom ASICs: all logic cells are pre-designed and some (possibly all) mask layers customized

Types of ASIC

- Full-custom ASICs: These ASICs are designed from scratch, offering maximum flexibility and performance but requiring significant time and resources.
- Semi-custom ASICs: Gate Array ASICs and Standard Cell ASICs provide a balance between customization and time-to-market. They utilize pre-designed blocks for certain functions while allowing customization for specific requirements.
- Programmable ASICs: FPGA (Field-Programmable Gate Array) and CPLD (Complex Programmable Logic Device) offer reconfigurable hardware, enabling rapid prototyping and design iteration.

Applications of ASIC

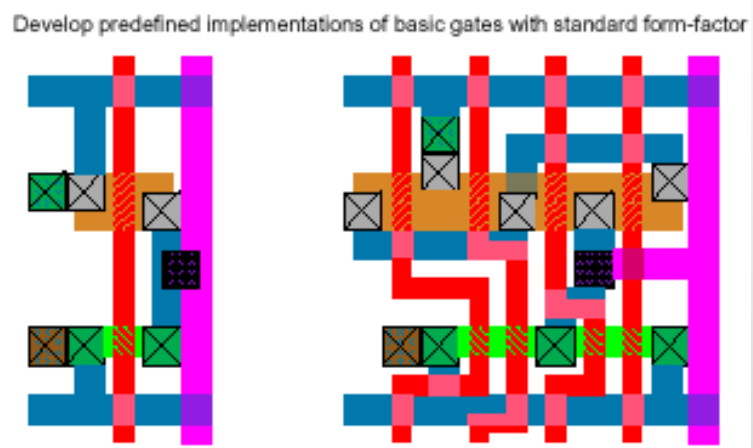
- Consumer electronics: ASICs power various devices such as smartphones, gaming consoles, and smart home appliances, providing optimized performance and power efficiency.
- Automotive industry: ASICs play a crucial role in automotive applications, including engine control units, infotainment systems, advanced driver-assistance systems (ADAS), and autonomous driving technology.
- Telecommunications: ASICs are integral to network infrastructure, facilitating high-speed data processing in switches, routers, and telecommunications equipment.
- Aerospace and defense: ASICs are used in radar systems, avionics, communication systems, and military-grade hardware, meeting stringent requirements for reliability, performance, and security.

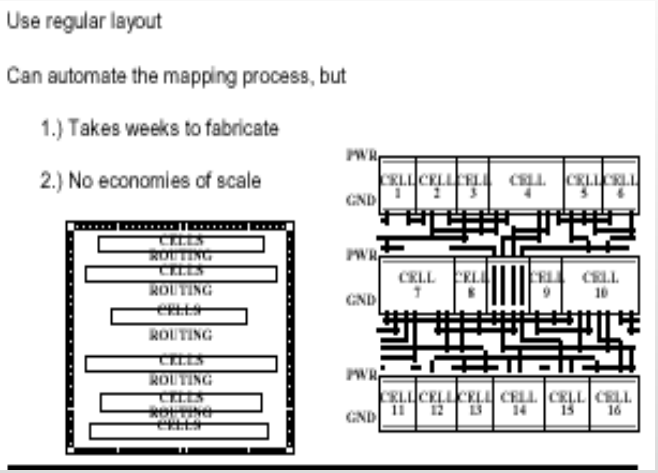
Full Custom ASIC

- A Full custom is one which includes some (possibly all) logic cells that are customized and all mask layers that are customized.
- A microprocessor is an example of a full-custom IC. Designers spend many hours squeezing the most out of every last square of microprocessor chip space by hand.
- Customizing all of the IC features in the allows designers to include analog circuits, optimized memory cells, or mechanical structures on an, for example. Full custom ICs are the most expensive to manufacture and to design.
- The specialized full-custom ICs are often intended for a specific application so, we might call some of them as full-custom ASICs.
- In a full-custom ASIC an engineer designs some or all of the logic cells, circuits, or layout specifically for one ASIC. This means the designer avoids using pretested and pre characterized cells for all or part of that design.

Semi-Custom ASICs

- Use logic blocks from standard cell libraries, other mega-cells, full-custom blocks, system-level macros(SLMs), functional standard blocks (FSBs), cores etc.
- Get all mask layers customized- transistors and interconnect
- Manufacturing lead time is around 8 weeks
- Less efficient in size and performance but lower in design cost





Gate Array Based ASIC

- This is a type of Semicustom ASICs.
- The transistors are predefined on the silicon wafer
- The predefined pattern of transistors on a gate array is the best array, and the smallest element that is replicated to make the base array is the base cell.
- Only top few layers of metal, which define the interconnect between transistors, are defined by the designer using custom masks. To distinguish this type of gate array from other types of gate array, it is often called a masked gate array(MGA).
- The logic cells in a gate-array library are often called macros. The reason for this is that the base-cell layout is the same for each logic cell, and only the interconnect is customized, which is similar to a software macro

Types of Gate-array based ASICs

- There are three types of Gate Array based ASICs.
- Channelled gate arrays.
- Channel less gate arrays.
- Structured gate arrays.

➢ Channelled gate arrays: The Channelled gate array was the first to be developed. In a channelled gate array space is left between the rows of transistors for wiring.

➢ Features of Gate-array based ASICs

- Only the interconnect is customized.
- The interconnect uses predefined spaces between rows of base cells
- Manufacturing lead time is between two days and two weeks,

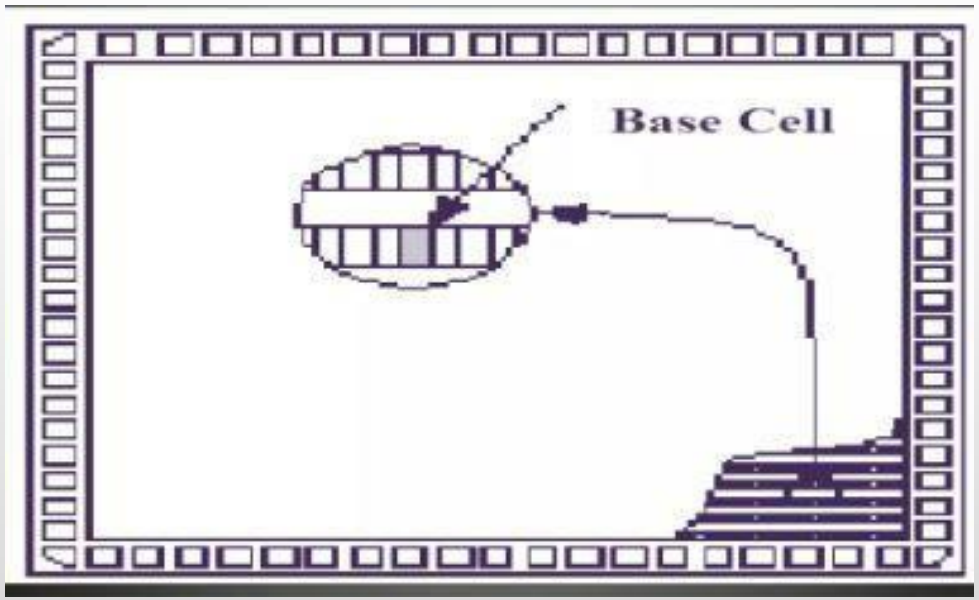


Fig: A channelled gate-array die

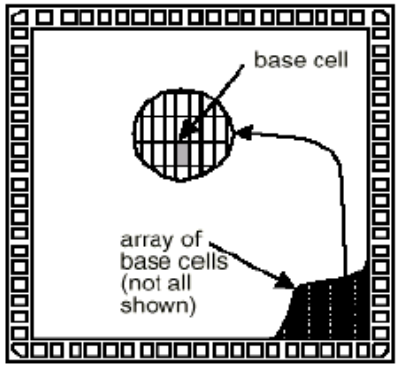
Channel less Gate Array

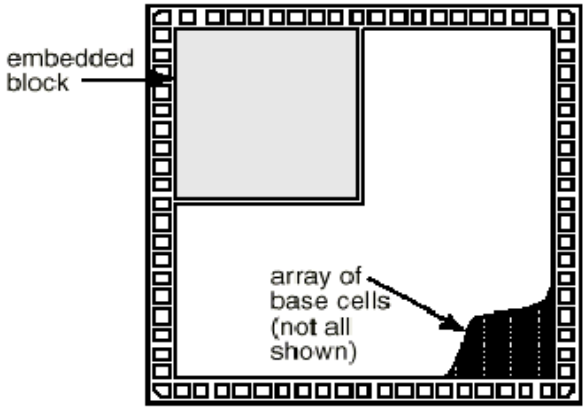
- This channel less gate-array architecture is now more widely used.; The routing on a channel less gate array uses rows of unused transistor.
  - The key difference between channel less and channelled gate array is there is no predefined areas set aside for routing between cells on a channel less gate array. Instead we route over the top of the gate array devices.
  - We can do this because we customize the contact layer that defines the connections between metal 1, the first layer of metal, and the transistors.

➢Features of Channel less Gate Array:

- Only the interconnect is customized
- Interconnect uses predefined spaces between rows of base cells.
- When we use an area of transistor for routing in a channel less array, we do not make any contacts to the devices lying underneath , we simply leave the transistors unused.

- A **channelless gate array** (**channel-free gate array**, **sea-of-gates array**, or **SOG** array)
  - Only some (the top few) mask layers are customized — the interconnect
  - Manufacturing lead time is between two days and two weeks.





- An **embedded gate array** or **structured gate array** (**masterslice** or **masterimage**)
  - Only the interconnect is customized
  - Custom blocks (the same for each design) can be embedded
  - Manufacturing lead time is between two days and two weeks.

- The basic difference between a channel less gate array and channelled gate array is that there are no predefined areas set aside for routing between cells on a channel less gate array. Instead we route over top of the gate array devices.

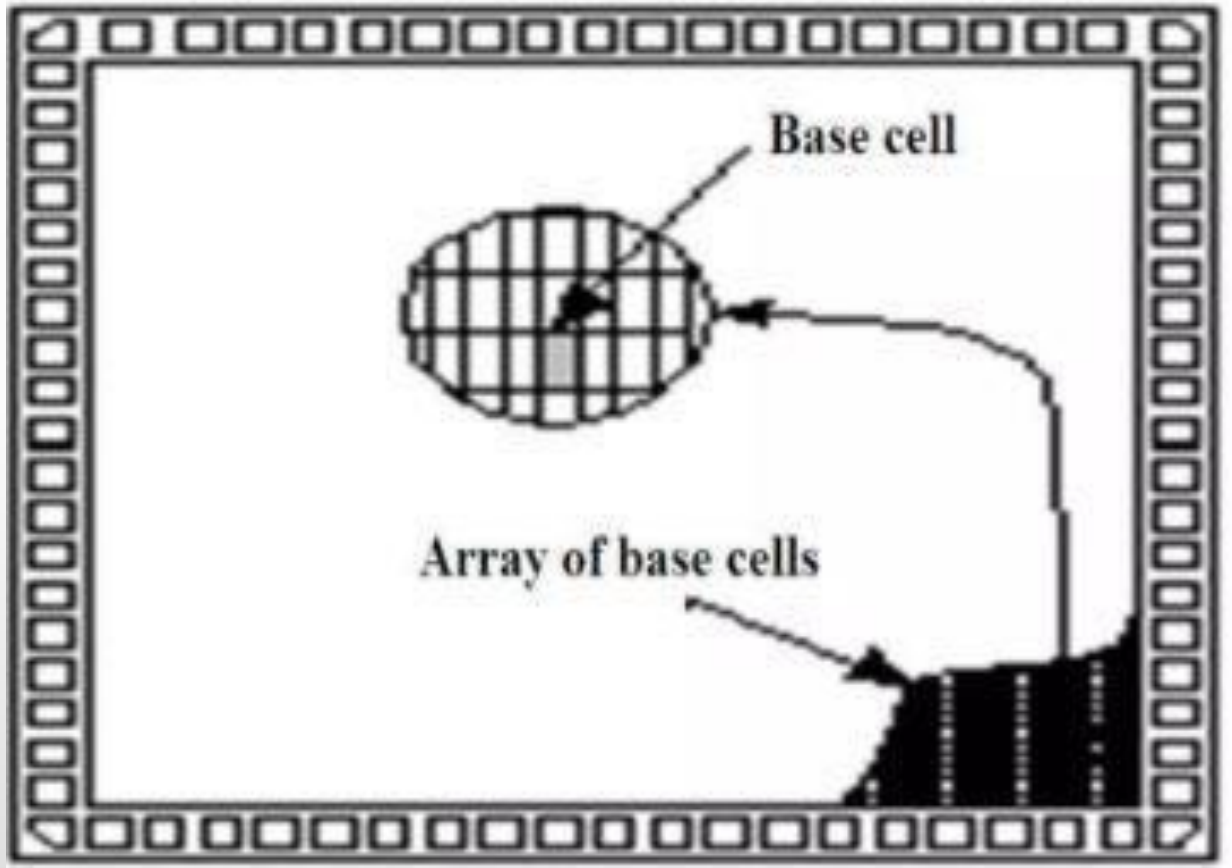


Fig: A channel less gate-array die

Structured Gate Array

- This design combines some of the features of Cell based ASIC(CBICs) and MGAs(Masked Gate Array) .It is also known as embedded gate array or structured gate array or master slice or also called as master image.
- One of the limitations of the MGA is the fixed gate array base cell. This makes the implementation of memory, difficult and inefficient.
- In an embedded gate array some of the IC area is set aside and dedicate it to a specific function. This embedded area either can contain a different base cell that is more suitable for building memory cells, or it can contain a complete circuit block, such as a microcontroller.

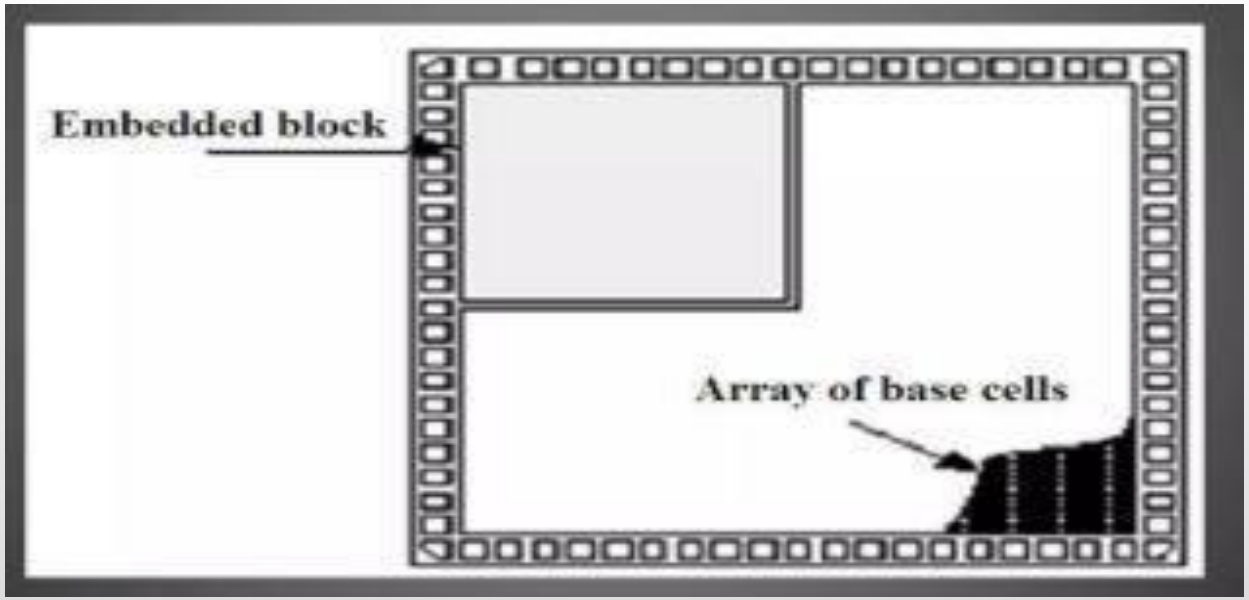


Fig: A structured or embedded gate-array die showing an embedded block in the upper left corner

Features of Structured Gate Array

- Only the interconnect is customized.
- Custom blocks (the same for each design) can be embedded.
- An embedded gate array gives the improved area efficiency and increased performance of a CBIC but with the lower cost and faster turn around of an MGA.
- The disadvantage of an embedded gate array is that the embedded function is fixed.

Advantages of ASICs

- Performance optimization: ASICs are custom-tailored to meet specific performance requirements, offering higher speed and efficiency compared to off-the-shelf solutions.
- Cost-effectiveness for high-volume production: While ASIC development incurs initial costs, it becomes cost-effective for high-volume production due to reduced per-unit costs.
- Reduced power consumption: ASICs are optimized for power efficiency, making them suitable for battery-powered devices and energy-conscious applications.
- Size and weight reduction: ASICs integrate multiple functions into a single chip, reducing the overall size and weight of electronic devices.
- Enhanced security features: ASICs can implement advanced security features such as hardware encryption, secure boot, and tamper resistance, providing robust protection against security threats.

Challenges in ASIC Design

- Complexity management: ASIC designs are becoming increasingly complex, requiring sophisticated design methodologies and tools to manage complexity effectively.
- Time-to-market constraints: Meeting tight deadlines while ensuring design quality poses a significant challenge in ASIC development, necessitating efficient design flows and project management.
- Verification and testing: Ensuring the correctness and reliability of ASIC designs through comprehensive verification and testing is crucial but time-consuming.
- Cost considerations: ASIC development involves substantial upfront costs, including design, fabrication, and testing expenses, which must be carefully managed to ensure project viability.

Future Trends in ASIC Technology

- Integration of AI and machine learning algorithms: ASICs are increasingly incorporating specialized hardware accelerators for AI and machine learning tasks, enabling efficient inference and training in edge devices.
- Advanced process nodes: Continued advancements in semiconductor manufacturing technologies, such as 7nm, 5nm, and beyond, enable higher transistor densities and improved performance for future ASIC designs.
- Increased focus on security features: With growing concerns about cybersecurity, future ASICs will integrate enhanced security features to protect against hardware-level attacks and data breaches.

Heterogeneous integration: ASICs will be increasingly integrated with other technologies such as MEMS (Micro-Electro-Mechanical Systems) and photonics to enable new functionalities and applications.

Thank You